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EXAMINER	
PHAM, TAMMY T	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/664,912	KIM ET AL.	
	Examiner	Art Unit	
	TAMMY PHAM	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,8,9,11,12,14-27,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,8,9,11,12,14-27,29,30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 23 April 2009 has been entered.

Response to Amendment

2. Claims 2, 4-7, 10, 13, 28, 31-47 have been cancelled. Independent claims 1, 3, 9, 30 have been amended. Claims 1, 3, 8-9, 11-12, 14-27, 29-30 are pending.

Response to Arguments

3. Applicant's arguments filed 23 April 2009 have been fully considered, as follows:

4. **In regards to independent claims 1, 9, 30,** Applicant's main argument is that the cited art of record fails to teach upon the newly amended claim language. However, this is not persuasive. Because, as analyzed below, the prior art of record continues to read upon the claim limitations as currently recited.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 3, 8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. **In regards to independent claim 1,** the amended claim language now recites of *"a second multiplexer part for simultaneously outputting the buffered pixel signals from the output buffer."* However, there is no support for this in the original disclosure. In particular, Applicant does not teach of the buffered signals going into the second multiplexer. Instead, Applicant teaches and there is only support for the second multiplexer (Fig. 4, item 272) inputting signals into the buffer (Fig. 4, items B1-B4). Appropriate correction is necessary.

7. **In regards to independent claim 9,** the amended claim language now recites of **"***a discharging part simultaneously outputting the pixel signals held in the holding part for the first horizontal period to corresponding data lines for an enable period of a source output enable signal of a second horizontal period and outputting a reference voltage to the corresponding data lines for a disable period of the source output enable signal of the second horizontal period."* However, there is no support for this in the original disclosure. Appropriate correction is necessary.

8. **In regards to claims 3, 8, 11-12, 14-27, 29,** these claims are being rejected for being dependents upon improper claims 1 and 9.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 3, 8-9, 11-12, 14-27, 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cairns et al. ("Cairns1") (US Patent Application: 2002/0030653 A1) in view of Cairns et al. ("Cairns2") (US Patent No: 6,268,841 B1), Enami et al (US Patent No: 5,892,493), Morita (US Patent No.: 6,989,810 B2) and Nitta et al. (U.S. Patent No.: 6,661,402 B2).

10. **As for independent claims 1, 30,** Cairns1 teaches of a data driving apparatus (Fig. 1, item 2) for a liquid crystal display device (Fig. 1), comprising:

11. a shift register part (Fig. 4, item 10) sequentially shifting an input source start pulse in accordance with an input source shift clock to generate a sampling signal;

12. a latch part (Fig. 4, item 11) sequentially latching a plurality of digitally pixel data in response to the sampling signal from the register part (Fig. 4, item 10);

13. a first multiplexer (Fig. 4, item 13) part performing a time-division on digital pixel data from the latch part;

14. a digital-analog converter (Fig. 4, item 12);

15. a demultiplexer (Fig. 4, item 14) part supplying the analog pixel signals from the digital-analog converter (Fig. 4, item 12) part to a plurality of output channels (section [0015]); and of providing signals for the enable period of a source output enable signal and a reference voltage of liquid crystal cells for the disabled period of the source output enable signal (Fig. 2); and

16. an output part (Fig. 4).

17. Cairns1 fails to teach of a shift register;

18. that the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data;

19. a positive digital-analog converter converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal;

20. a negative digital-analog converter converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal;

21. supplying the positive pixel signal from the positive digital-analog converter and the negative pixel signal from the negative digital-analog converter to corresponding output channels;

22. a sampling part sampling the positive pixel signals and the negative pixel signals from the demultiplexer;

23. a holding part holding the sampled pixel signals from the sampling part, and

24. an output buffer part for buffering the held pixels signals from the holding part, and

25. a second multiplexer part for simultaneously outputting the buffered pixel signals from the output buffer part in response to a source output enable signal during the next horizontal period following the horizontal period;

26. wherein the device is controlled by an ODD/EVEN signal which performs the time-division for a horizontal period.

27. Cairns1 explicitly teaches of a shift register in another embodiment (Fig. 8).

28. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the shift register of the other embodiment with Cairns since shift registers ensure that all of the flip flop circuits are able to reset to the "zero" logic state before operation (section [0058]).

29. Nitta teaches that the digital pixel data sequentially being outputted to positive and negative paths by unit of adjacent digital pixel data (Fig. 2);

30. a positive digital-analog converter (Fig. 2, item 228) converting one digital pixel data of the adjacent digital pixel data inputted to the positive path into a positive pixel signal;

31. a negative digital-analog converter (Fig. 2, item 229) converting the other digital pixel data of the adjacent digital pixel data inputted to the negative path into a negative pixel signal;

32. supplying the positive pixel signal from the positive digital-analog converter (Fig. 2, item 228) and the negative pixel signal from the negative digital-analog converter (Fig. 2, item 229) to corresponding output channels; and

33. a second multiplexer part (Fig. 2, item 233) for simultaneously outputting the buffered pixel signals from the output buffer part (Fig. 2, item 231).

34. It would have been obvious to one with ordinary skill in the art at the time the invention was made to incorporate the concept of combining the separate the signals in accordance to their polarity as taught by Nitta with the driving circuitry of Cairns1 and Cairns2 in order to improve the picture quality by providing a more efficient driving method (Nitta, column 1, lines 50-55).

35. Cairns2 teaches of a sampling part (Fig. 11b, items 47, 49) sampling the pixel signals from the demultiplexer output channels (Fig. 11b, section "output from demultiplexer");

36. a holding part (Fig. 11b, items C1-C2) holding the sampled pixel signals from the sampling part (Fig. 11b, items 47, 49), providing the corresponding data lines (Fig. 11b, item 8) with the pixel signals from the output buffer part (Fig. 11b, item 40);

37. an output buffer part (Fig. 11b, item 40) for buffering the held pixels signals from the holding part (Fig. 11b, items C1-C2); and

38. wherein the device is controlled by an ODD/EVEN signal which performs the time-division for a horizontal period (column 8, lines 20-30).

39. It would have been obvious to one with ordinary skill in the art at the time the invention was made to combine the output part of Cairns2 with the rest of the components of the data driving apparatus of Cairns1 in order to have fewer converters (Cairns2, column 4, lines 33-35).

40. Cairns1 and Cairns2 fails to teach of a second multiplexer part.

41. Enami teaches of a second multiplexer part (Fig. 1, item 38) for simultaneously outputting the sampled pixel signals from the output buffer part (Fig. 8b, items 40) in response to a source output enable signal.

42. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a second multiplexer as taught by Enami with the data driver of Cairns1 and the output part of Cairns2 in order to allow the apparatus to perform multiplex driving in which the data voltage is sequentially applied to a number of data lines in each of the data groups (Enami, column 3, lines 49-51).

43. Cairns1, Cairns2, and Enami fails to teach that the signals are separately being supplied during the first half of the horizontal period and during the second half of the horizontal period.

44. Morita teaches that the signals are separately being supplied during the first half of the horizontal period (Fig. 8, items t2-t7) and during the second half of the horizontal period (Fig. 8, items t8-t13, column 8, lines 18-28).

45. It would have been obvious to one with ordinary skill in the art at the time the invention was made have the signals be supplied separately as taught by Morita with the data driving apparatus of Cairns1, the output part of Cairns2, and the second multiplexer part of Enami. The

benefits of separating supplying the signals in the first and second horizontal period, is that it allows for a more simple data structure (Morita, column 3, lines 67-1).

46. **As for independent claim 9,** in addition to the claim limitation of claim 1, Cairns1 teaches of performing a certain function for a plurality of data lines (Fig. 9) for a first horizontal period (Fig. 2);

47. of outputting one signal during the first horizontal period with an enabling signal and outputting a reference voltage during a second horizontal signal with a disable period; and

48. of the demultiplexer (Fig. 6, item 14) corresponding to the data lines (Fig. 6).

49. Cairns1 fails to teach of a level shifter part raising a voltage of the data;

50. a discharging part simultaneously outputting the pixel signals held in the holding part for the first horizontal period to corresponding data lines for an enable period of a source output enable signal of a second horizontal period and outputting a reference voltage to the corresponding data lines for a disable period of the source output enable signal of the second horizontal period.

51. Cairns1 explicitly teaches of a shift register in another embodiment (Fig. 8).

52. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the shift register of the other embodiment with Cairns since shift registers

ensure that all of the flip flop circuits are able to reset to the "zero" logic state before operation (section [0058]).

53. Enami teaches of a discharging part (Fig. 1, item 38) simultaneously outputting the pixel signals held in the holding part for the period to corresponding data lines for an enable period of a source output enable signal (Fig. 1, outputs of item 40) of a second period and outputting a reference voltage (Fig. 1, outputs of item 38) to the corresponding data lines (Fig. 1, items d1A-dnD).

54. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include a discharging part as taught by Enami with the data driver of Cairns1 and the output part of Cairns2. The benefit of this combination is to allow the apparatus to perform multiplex driving in which the data voltage is sequentially applied to a number of data lines in each of the data groups (Enami, column 3, lines 49-51).

55. **As for claim 3,** Cairns1teaches that the digital-analog converter part (Fig. 4, item 12, section [0019]) and a demultiplexer part (Fig. 4, item 14, section [0016]).

56. Cairns1 fails to teach of a second multiplexer part.

57. Cairns2 teaches of a second multiplexer part (Fig. 11b, items 47, 49, column 10, lines 9-12).

58. It would have been obvious to one with ordinary skill in the art at the time the invention was made to include the second multiplexer of Cairns2 with the DAC of Cairns1 in order to

provide the apparatus with a data line driver where there are more data lines than data line circuits (Cairns2, column 4, lines 21-25).

59. **As for claim 8,** Cairns1 as modified by Cairns2 and Enami teaches that the sampling switches controlled by an ODD/EVEN signal which performs the time-division on a horizontal period (Cairns2, column 1, lines 54-58).

60. **As for claim 11,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part (Cairns1, Fig. 4, item 13) comprises:

61. a plurality of positive path switches coupled to input channels for the pixel data and commonly connected to the positive polarity output channel; and

62. a plurality of negative path switches coupled to the input channels for the pixel data, connected to the positive path switches in parallel, and commonly connected to negative polarity output channel (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

63. **As for claim 12,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the demultiplexer (Cairns1, Fig. 4, item 14) part comprises: a plurality of positive path switches forming a plurality of different positive paths corresponding to the data lines, and commonly connected to a positive digital-analog converter, and a plurality of negative path switches forming a plurality of different negative paths, commonly connected to a negative digital-analog converter (Id.), wherein the negative path switches are connected to the positive path switches in

parallel (Cairns1, Fig.4, section [0015]) (Nitta, Fig. 1, column 3, lines 23-33; column 4, lines 35-30).

64. **As for claim 14,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling part (Cairns2, Fig. 11b) and the holding part sample and hold the pixel signals supplied for the next horizontal period through the channel different from that of the pixel signal supplied for the first horizontal period (Cairns2, Fig. 12, each column has at least three sets of buffers).

65. **As for claim 15,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the sampling part (Cairns2, Fig. 11b) has a second demultiplexer (Cairns2, Fig. 3, item 25) part comprising; a plurality of the positive path switches forming a plurality of different positive paths and connected to the output channels of the demultiplexer part (Id.); and a plurality of negative path switches forming a plurality of different negative paths and connected to the output channels of the demultiplexer part (Id.) (Cairns2, Fig. 12, column 10, lines 18-41) (Nitta, Fig. 2, column 3, lines 23-33; column 4, lines 35-30).

66. **As for claim 16,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the holding part comprises:

67. positive path capacitors charging and holding the positive pixel signals from the positive path switches of the second demultiplexer (Cairns2, Fig. 3, item 25) part; and

68. negative path capacitors charging and holding the negative pixel signals from the negative path switches of the second demultiplexer (Id.) part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

69. **As for claim 17,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the discharging part comprises:

70. a second multiplexer part (Cairns1, Fig. 4, item 14) having:

71. a plurality of positive path switches connected to the positive path switches of the second demultiplexer (Cairns1, Fig. 4, item 14) through the holding part and connected to the data lines; and

72. a plurality of negative path switches connected to the negative switches of the second demultiplexer (Id.) through the holding part and connected to the data lines (column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}).

73. **As for claim 18,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer, the demultiplexer (Cairns2, Fig. 3, item 25), and the second demultiplexer (Id.) are controlled by a first control signal through an input polarity control signal and an ODD/EVEN signal performing the time-division on a horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

74. **As for claim 19,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal performsthe time-division on an enable period determined by a source output

enable signal for the horizontal period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

75. **As for claim 20,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the ODD/EVEN signal further performs the time-division on a disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

76. **As for claim 21,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the multiplexer part, the demultiplexer (14) part in Fig.4 and section [0015] {Cairns1} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}. The combination of Cairns2 and Nitta teaches that the second demultiplexer (64) part recharge the holding part with the pixel signals for the disable period, wherein the pixel signals are generated for a previous enable period in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

77. **As for claim 22,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the source output enable signal is generated by increasing the disable period of an external reference source output enable signal in order to secure a recharging period of the holding part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

78. **As for claim 23,** Cairns1 as modified by Cairns2, Enami and Nitta teaches the second multiplexer part is controlled by the first control signal and a second control signal that is phase-inversed with respect to the first control signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

79. **As for claim 24,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that an output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signals discharged from the holding part to the discharging part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

80. **As for claim 25,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of positive path output buffers (Id.) connected between the positive path capacitors of the holding part and the positive path switches of the second multiplexer part; and a plurality of negative path output buffers (Id.) connected between the negative path capacitors of the holding part and the negative path switches of the second multiplexer part in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

81. **As for claim 26,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part buffering the pixel signal supplied through the output channels of the second multiplexer part and supplying the pixel signals to each of the data lines

in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

82. **As for claim 27,** Cairns1 as modified by Cairns2, Enami and Nitta teaches that the output buffer (Cairns2, Fig. 11b, item 40) part comprises: a plurality of output buffers (Cairns2, Fig. 11b, item 40) connected between the output channels of the second multiplexer part and the data lines in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

83. **As for claim 29,** Cairns1 as modified by Cairns2, Enami and Nitta teaches of: teaches that a third multiplexer part supplying the pixel signals from the output part to the corresponding data lines for the enable period of the source output enable signal and commonly supplying a reference voltage of the liquid crystal cells to the corresponding data lines for the disable period of the source output enable signal in Fig. 12 and column 10, lines 18-41 {Cairns2} and in column 3, lines 23-33; column 4, lines 35-30 and Fig. 2 {Nitta}.

Conclusion

84. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammy Pham whose telephone number is (571) 272-7773. The examiner can normally be reached on 8:00-5:30 (Mon-Fri).

85. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

86. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TP
22 June 2009

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